

PG410 A01

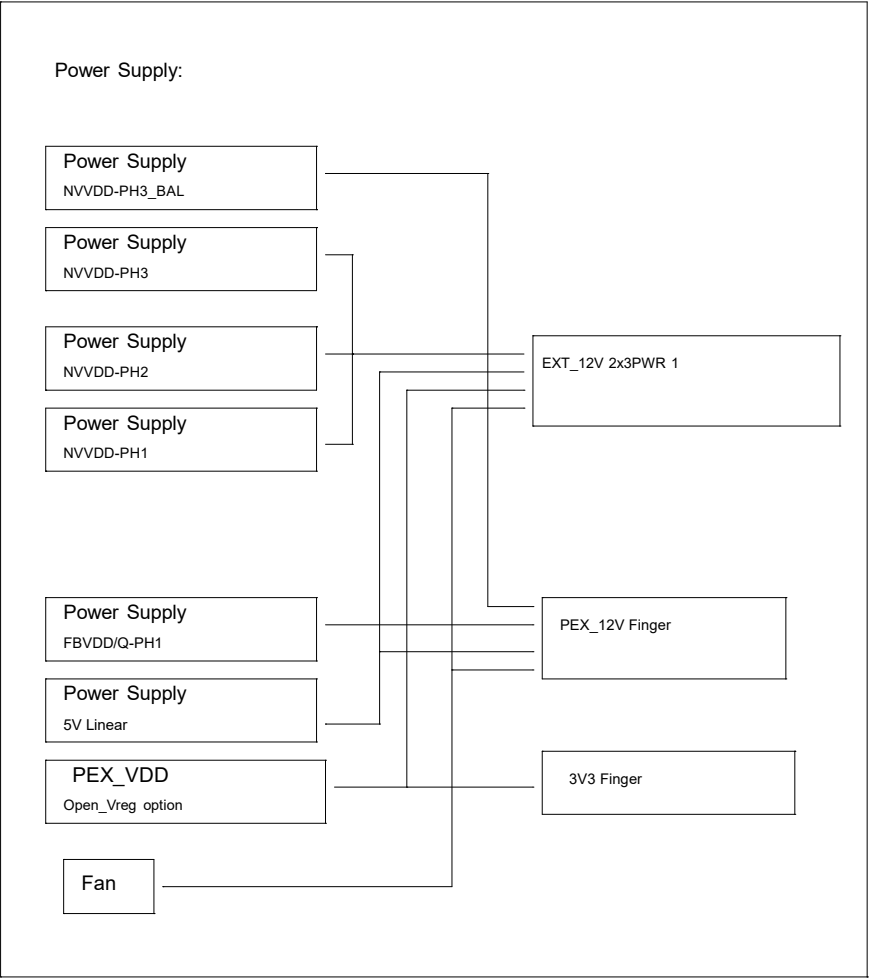
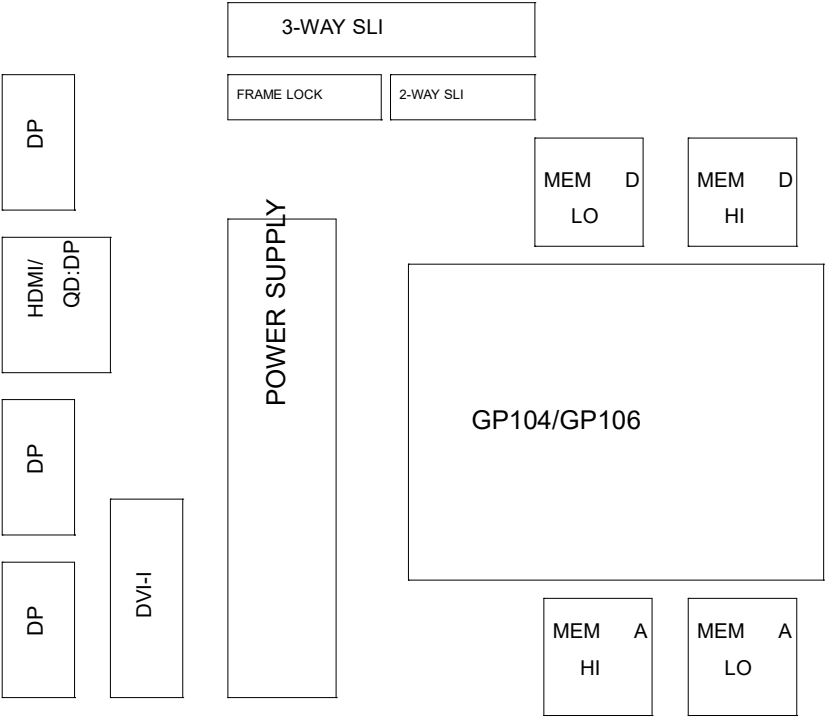
GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

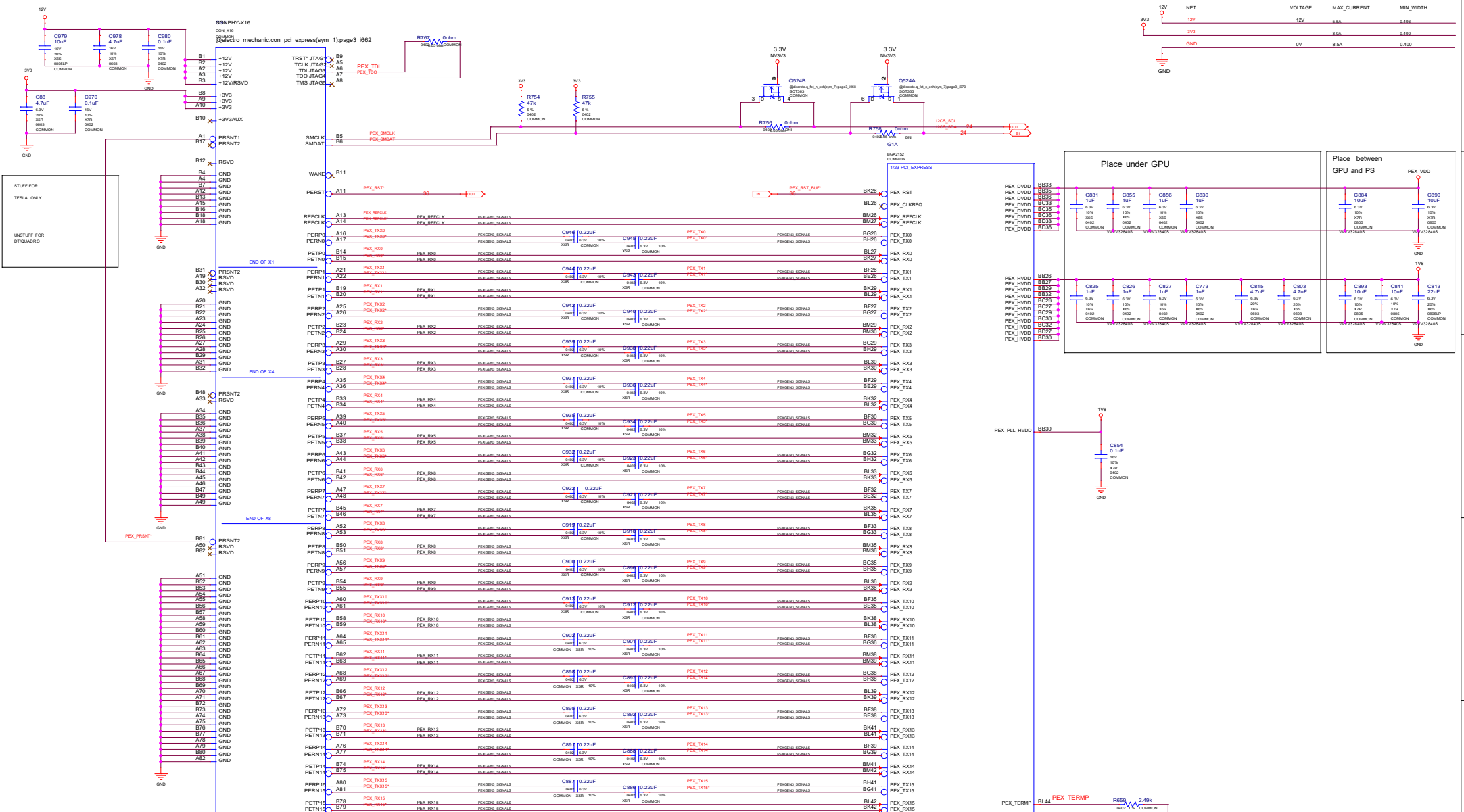
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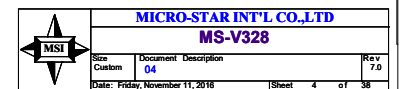
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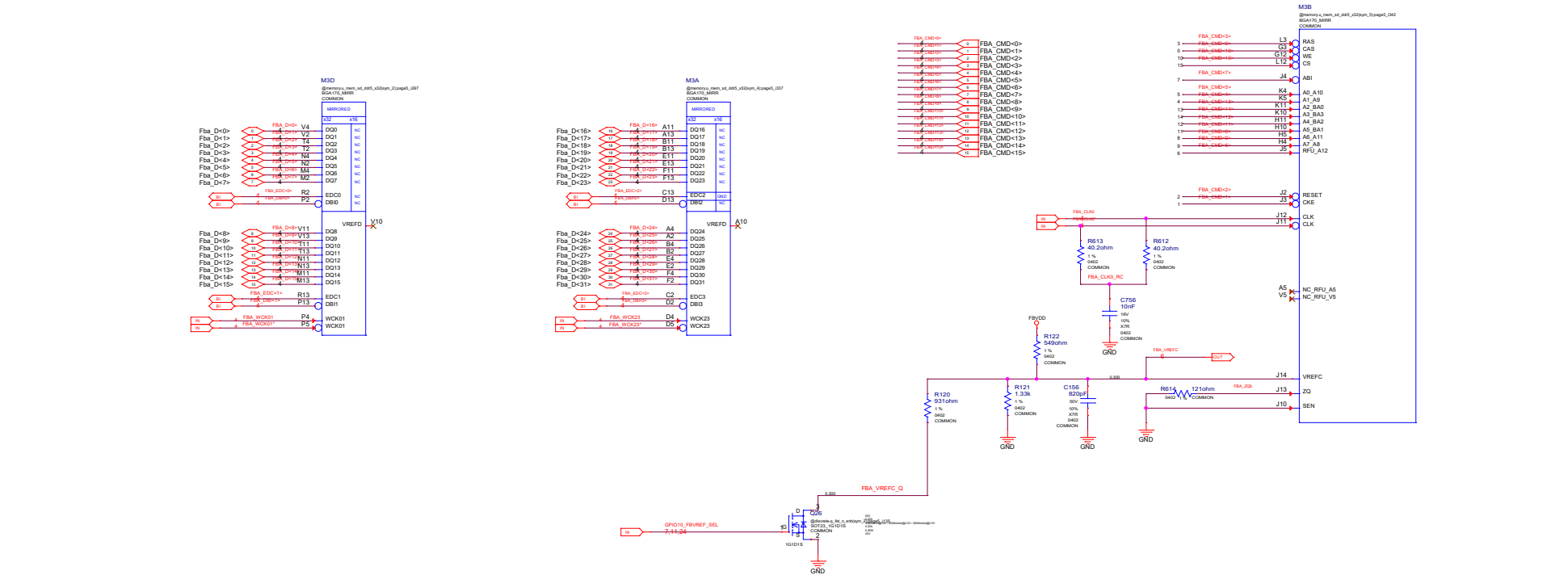
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26	PS: 1V8_PLL, 1V8_AON
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32	PS: NVVDD Rail Balance Login & Dynamic Phase
33	PS: Input, Filtering, and Monitoring
34	PS: 12V Power Steering,PSI Control & LED
35	PS: Shut Down and Sequencing
36	PS: GC6 MISC
37	MECH

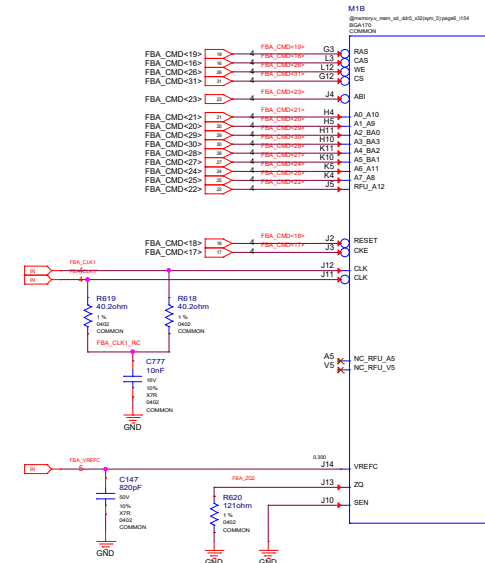
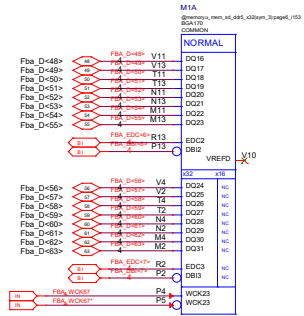
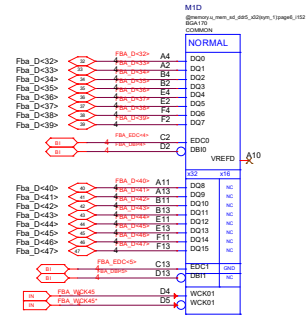
6.1 1. NVVDD_VR 2. L 3. C 4. HDMI D P CLAY



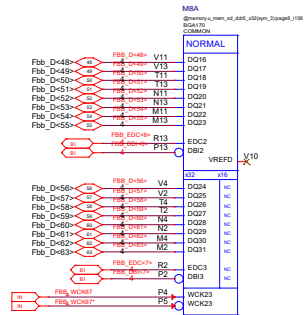


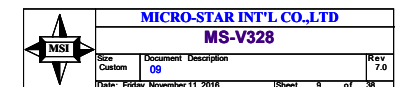
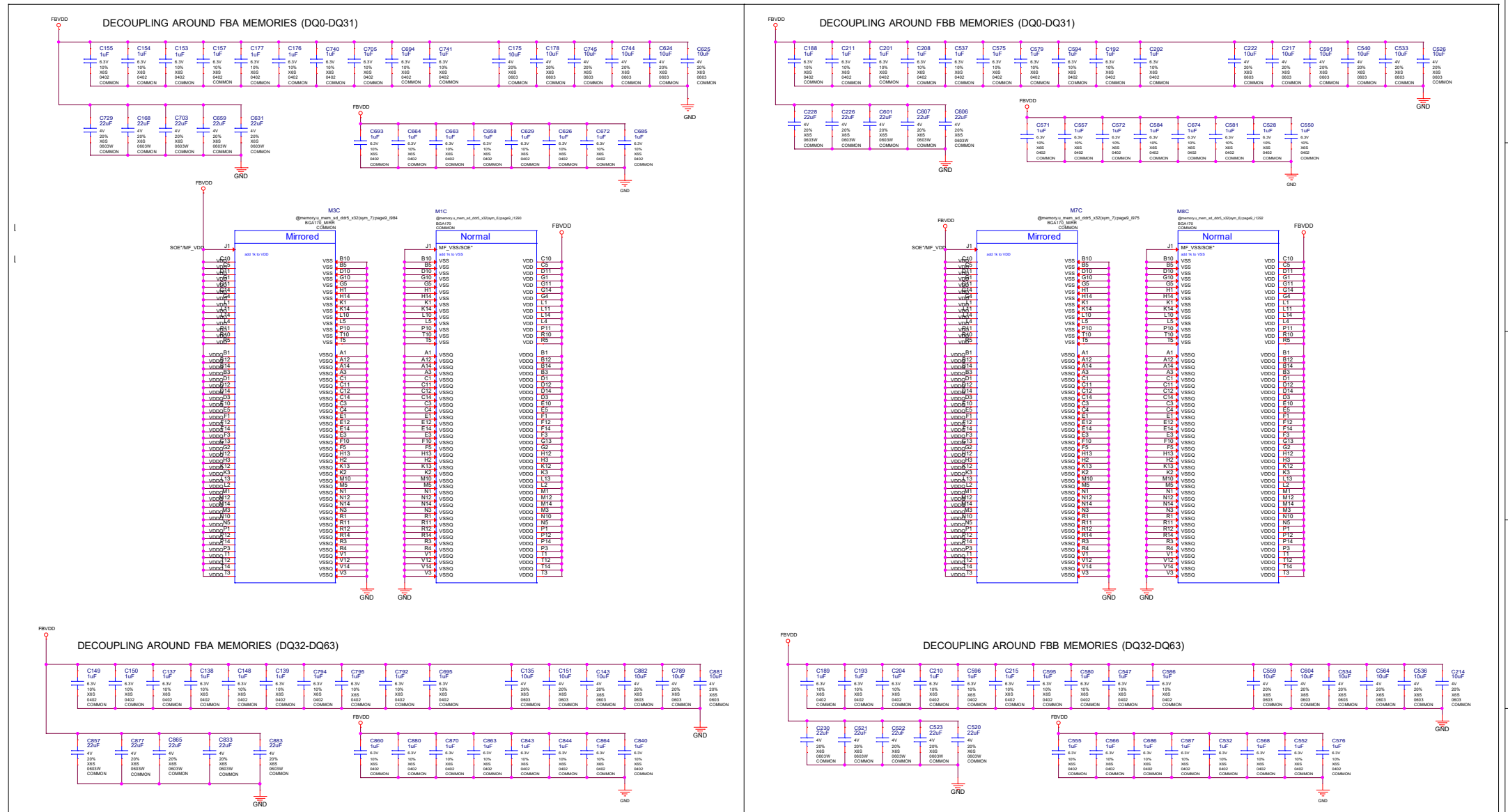






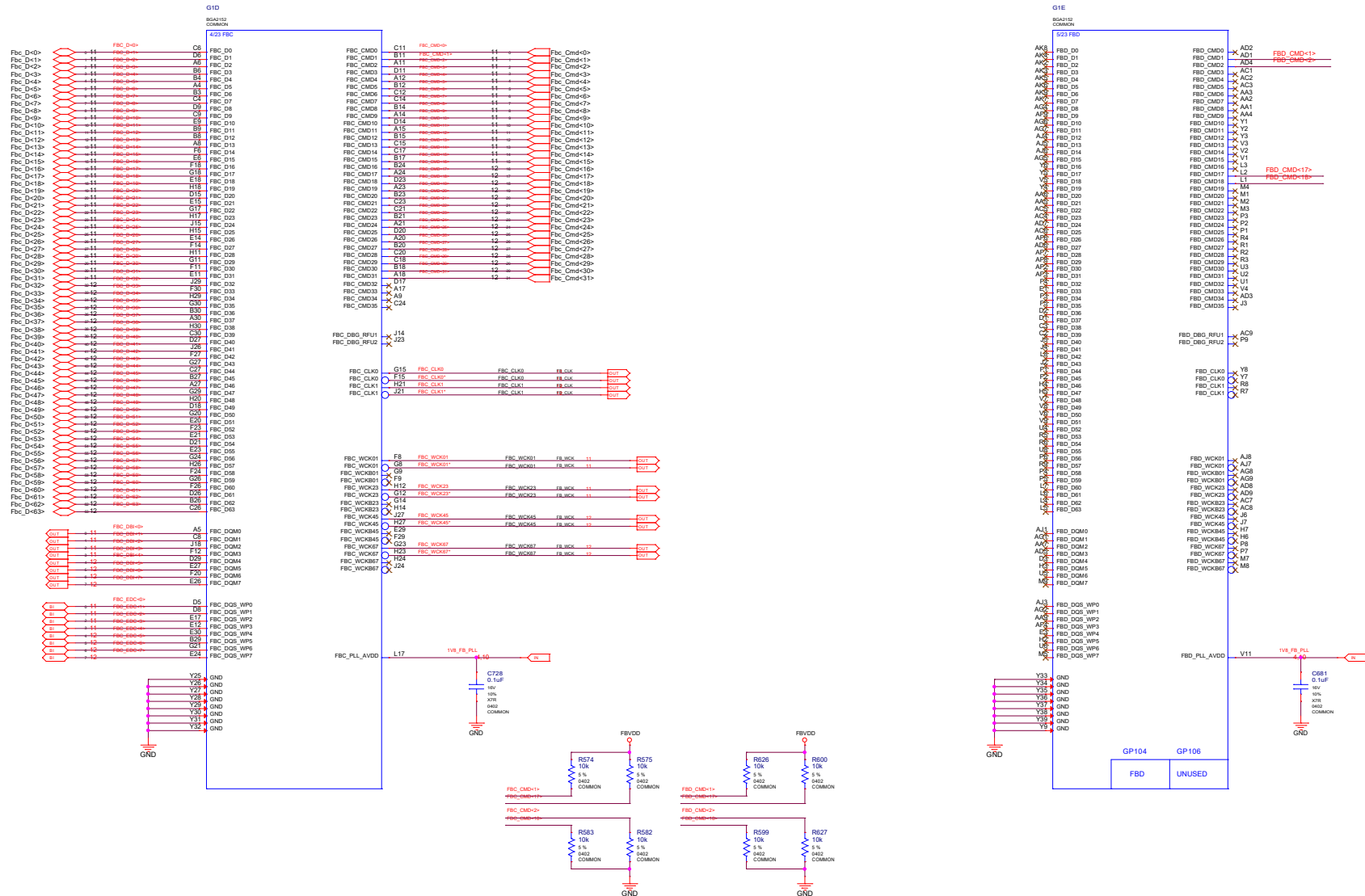


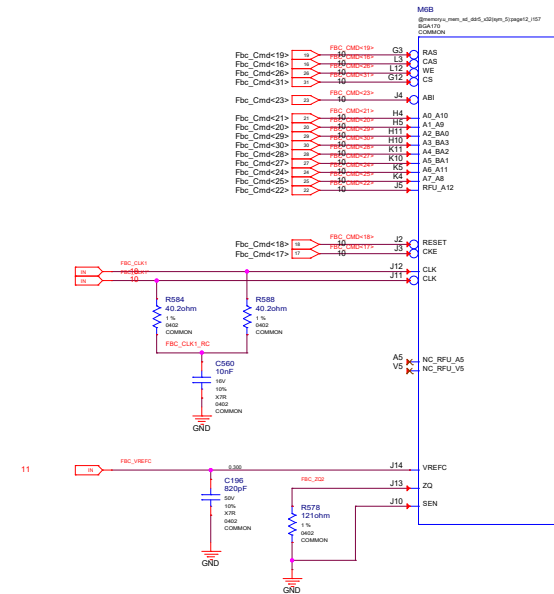
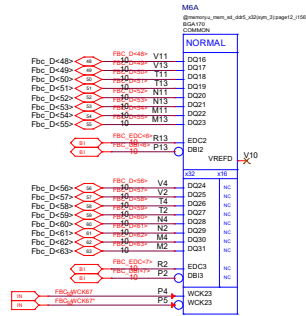
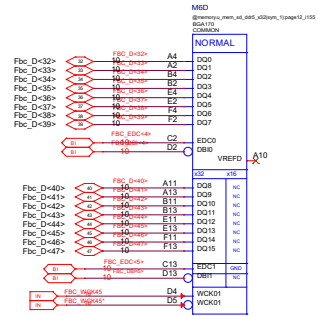





GDDR5 CMD Mapping


CMD	G_31	32-63
CM00	CAS*	
CM01	CKE*	
CM02	RS*	
CM03	RA*	
CM04	A1_A0	
CM05	A2_A10	
CM06	A12_RFU	
CM07	AB*	
CM08	AB_A11	
CM09	A7_A6	
CM10	WE*	
CM11	AS_BA1	
CM12	AS_BA2	
CM13	A2_BA0	
CM14	A3_BA3	
CM15	CS*	
CM16		CAS*
CM17		CKE*
CM18		RS*
CM19		RA*
CM20	A1_A0	
CM21	A6_A10	
CM22	A12_RFU	
CM23	AB*	
CM24	AB_A11	
CM25	A7_A6	
CM26	WE*	
CM27	AS_BA1	
CM28	AS_BA2	
CM29	A2_BA0	
CM30	A3_BA3	
CM31	CS*	



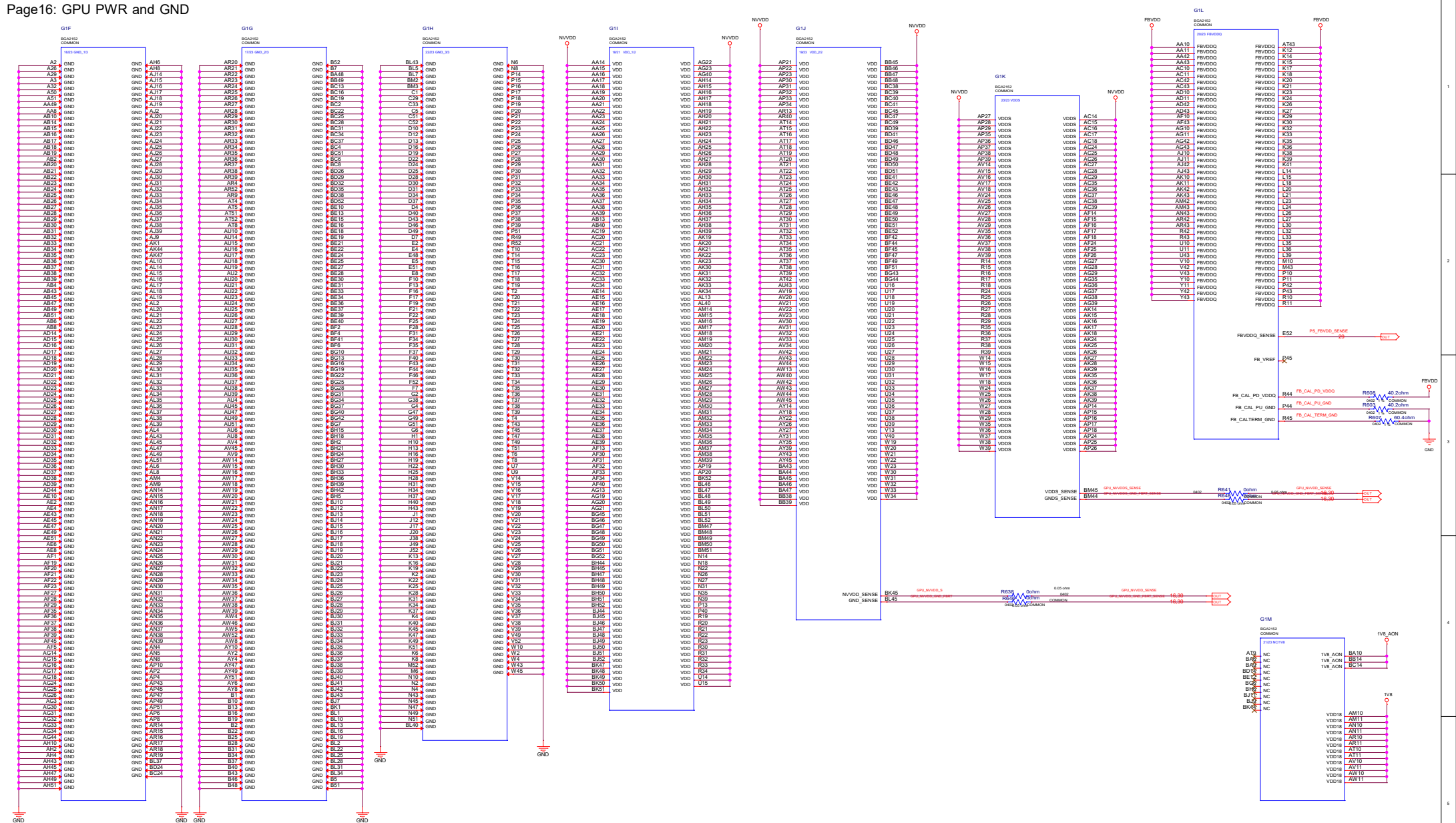




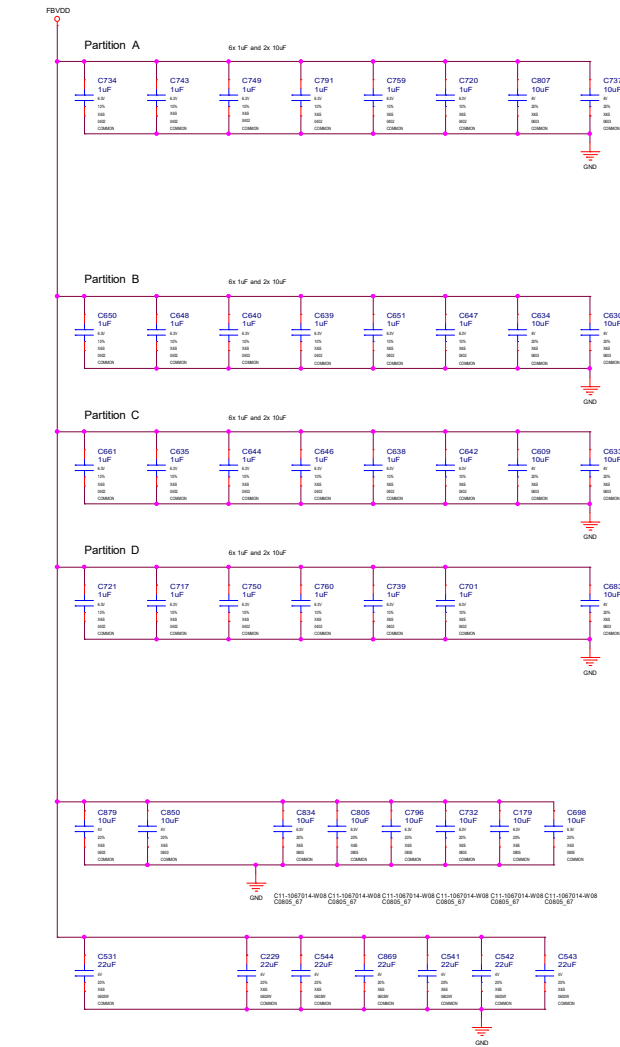
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MS-V328			
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Custom	13		7.0
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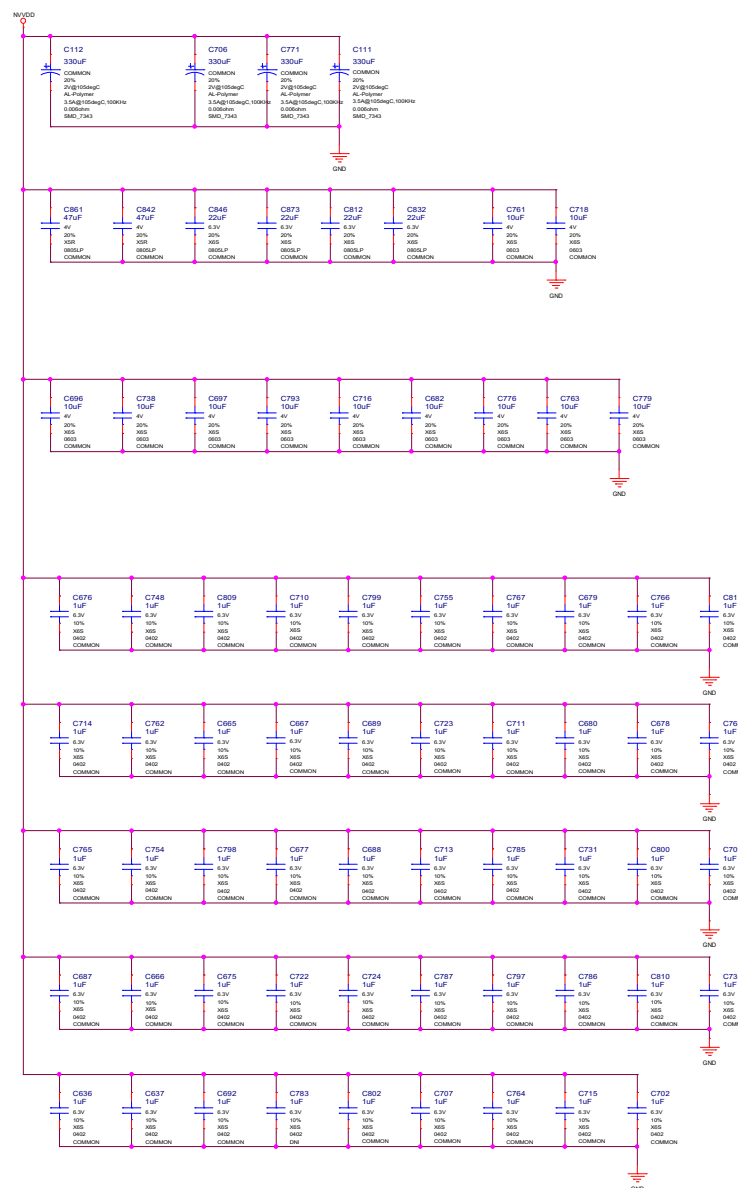
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MS-V328			
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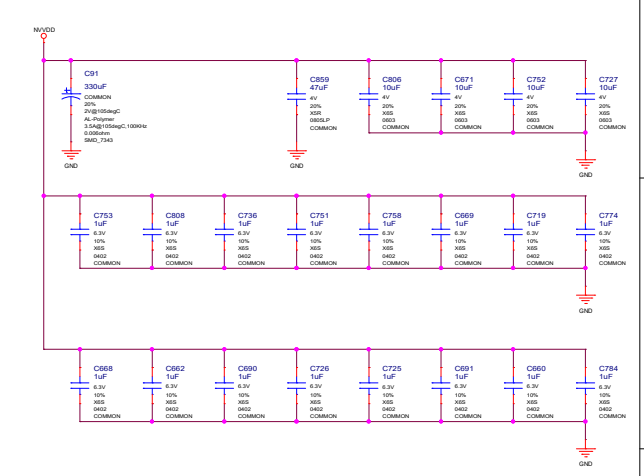
FBVDD



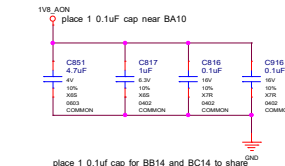
NVVDD



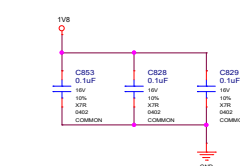
NVVDD

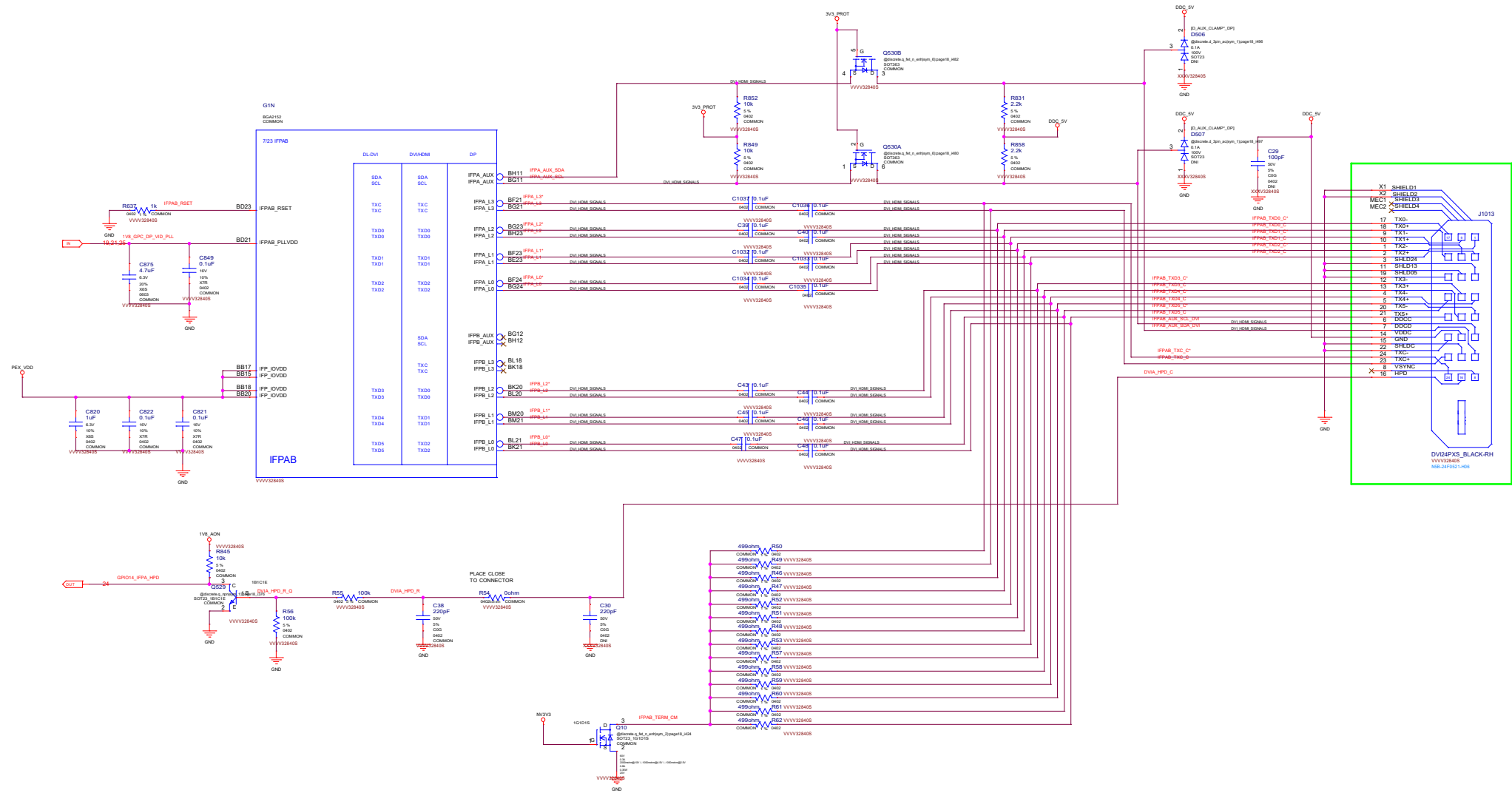


1V8_AON

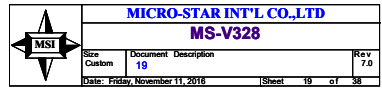
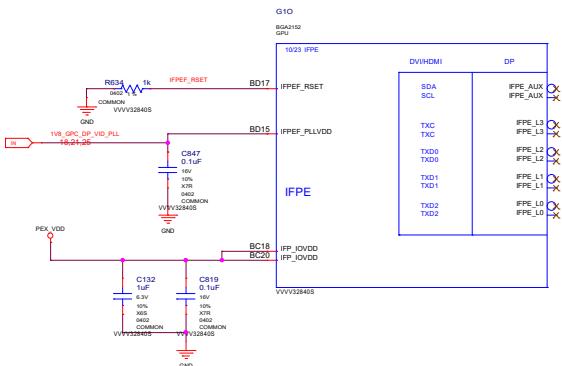


1V8_MAIN





更換為單層無架高



1

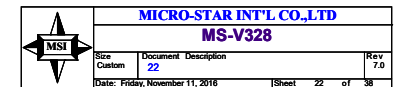
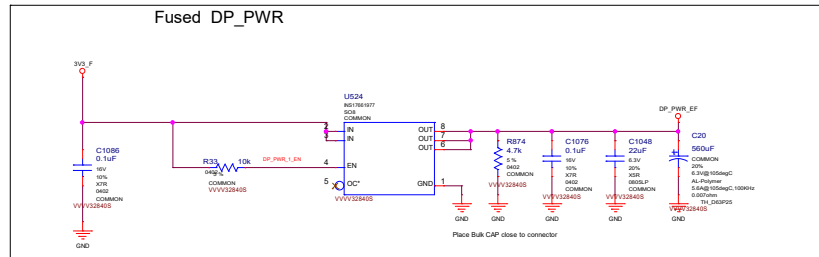
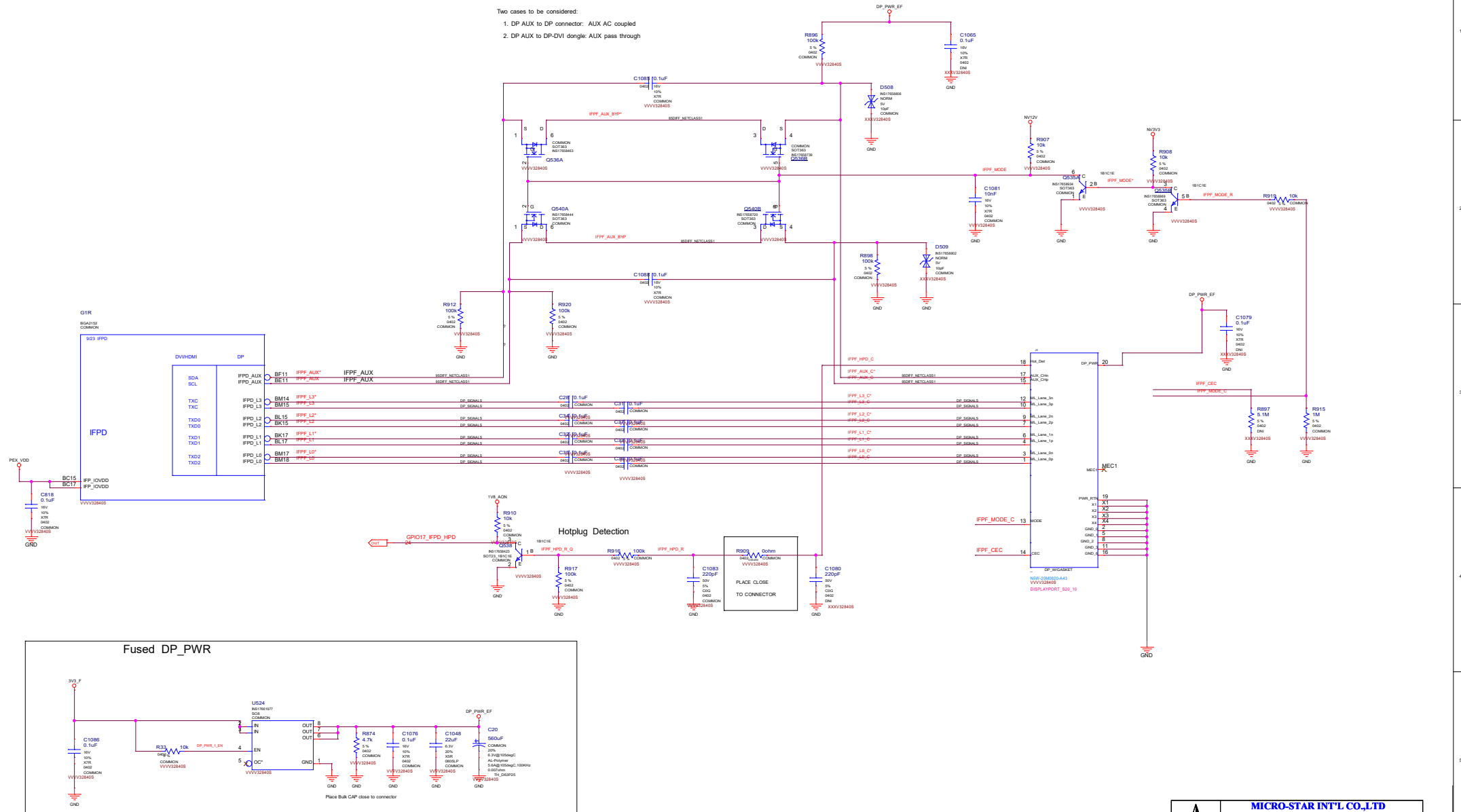


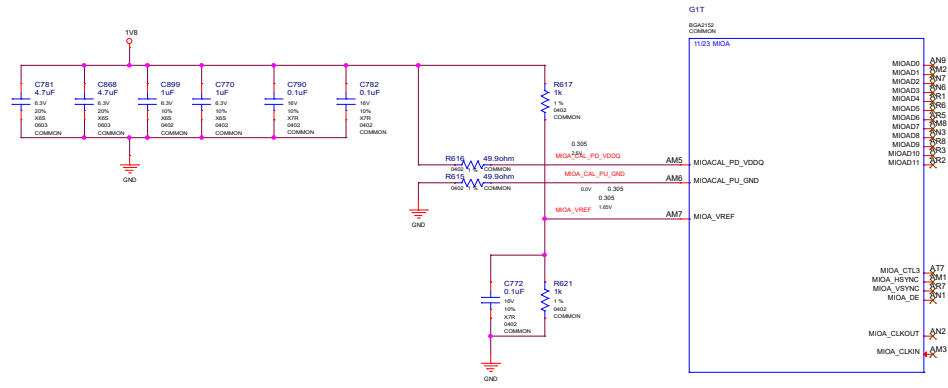
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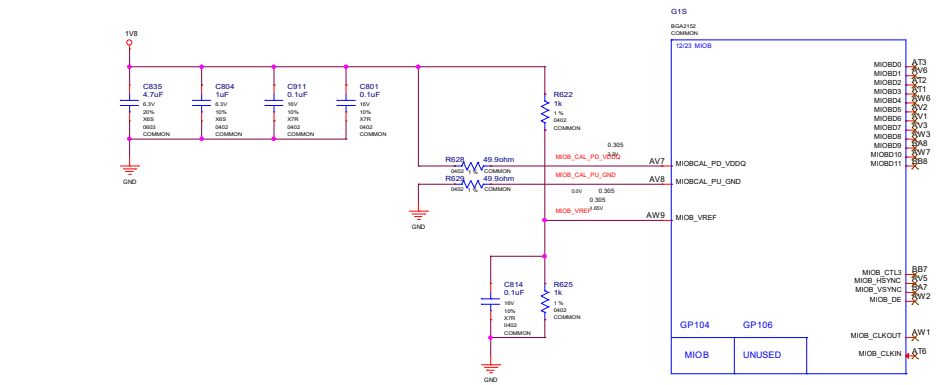
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





Pad Overlap R1042 & R1043



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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

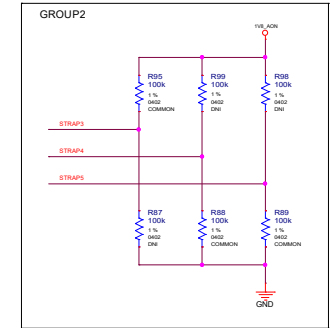
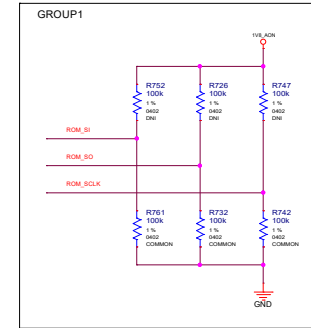
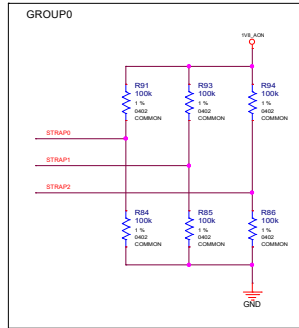
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

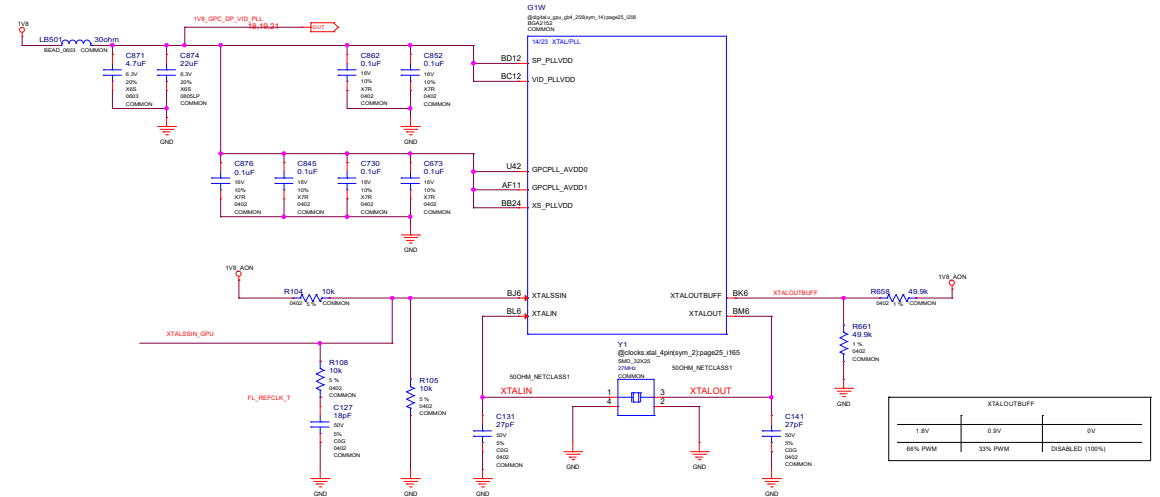
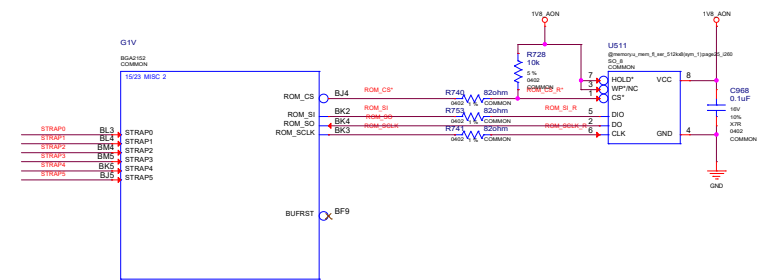
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[3:0]	Config	Width	Vendor
0000	256Mx32 256-bit	Samsung	
0001	256Mx32 256-bit	Micron	
0010	256Mx32 256-bit	Hynix	
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



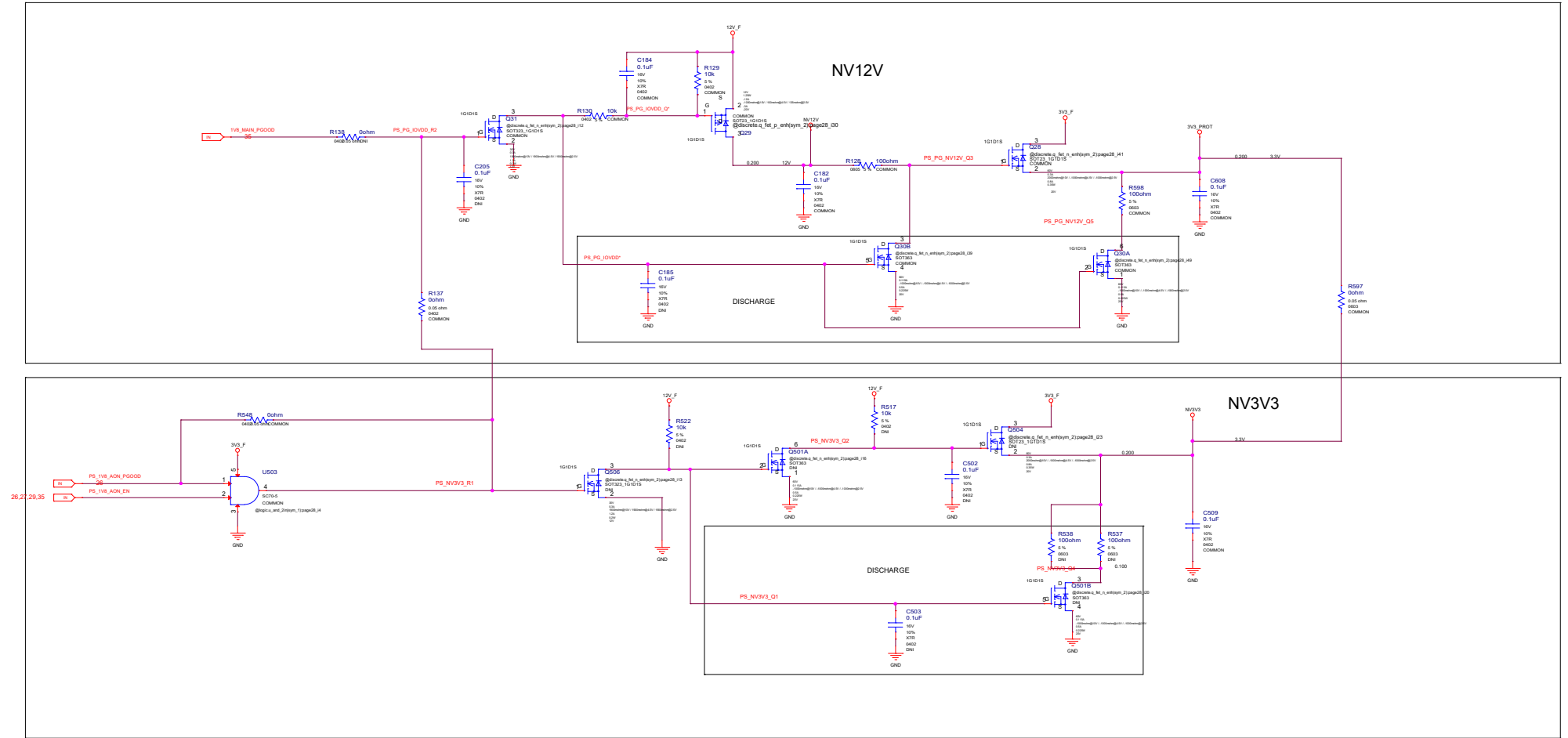
XTALOUTBUFF		
1.8V	0.9V	0V
88% PWM	33% PWM	DISABLED (100%)

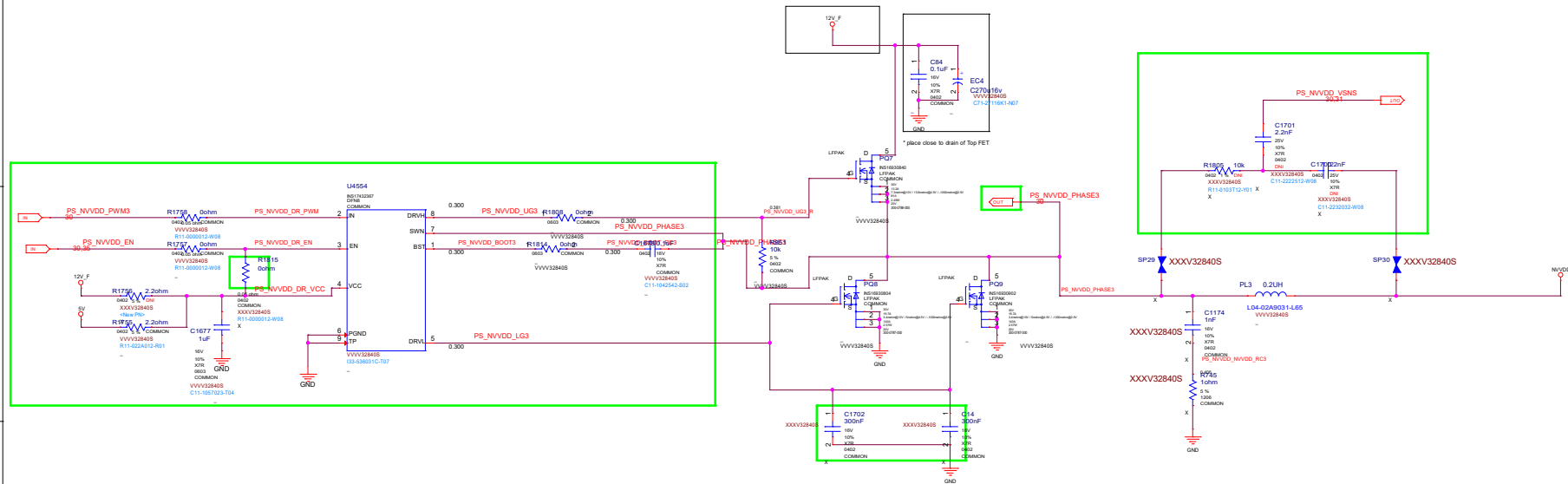


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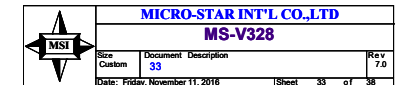
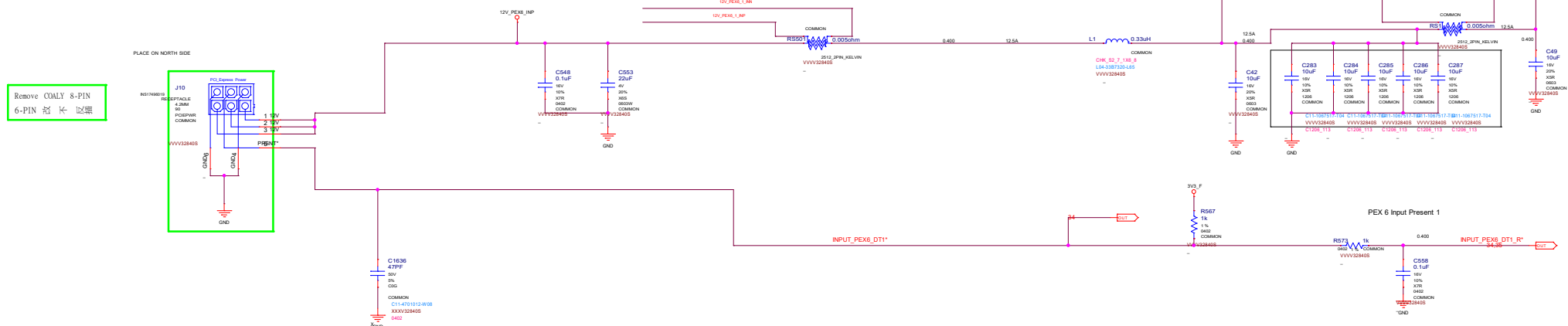
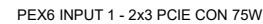
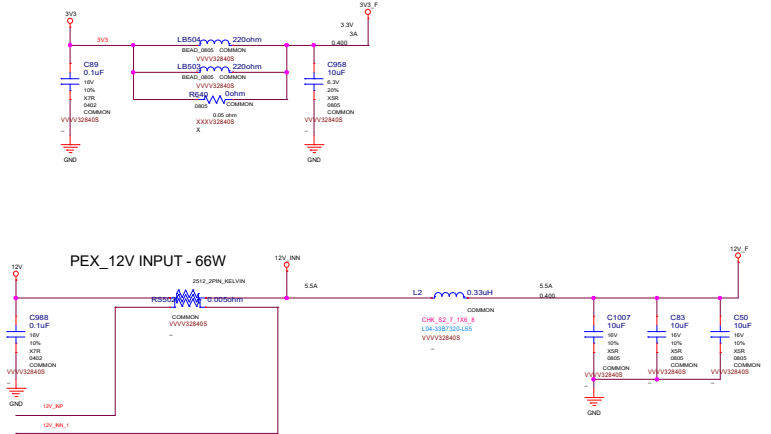
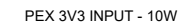
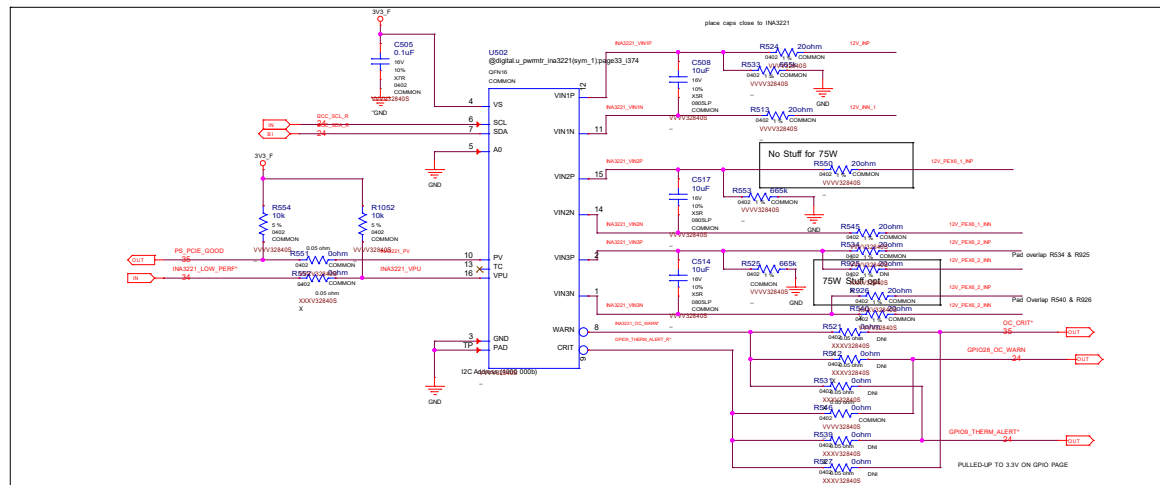


CORE 90A /3 =30A
CORE 1 - EXT 6
CORE 2 - EXT 6
CORE 3 - BUS
MEM 30A- BUS
-BUS WARRING-

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CORE 90A /4 =22.5A
CORE 1 - EXT 6
CORE 2 - EXT 6
CORE 3 - BUS
CORE 4 - EXT 6
MEM 30A- BUS

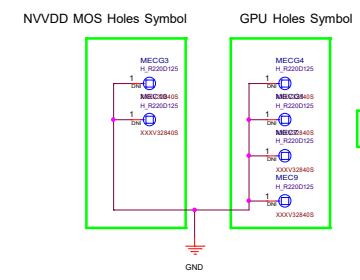
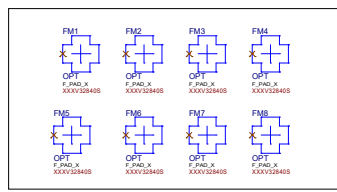
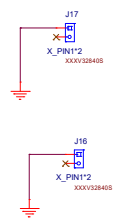
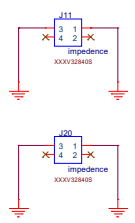
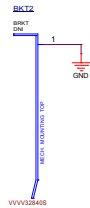
```



remove 5V LED NET

Brackets:



Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1

Page: 18	DVI-D 同 差 奇 偶 線 重 複
Page: 19	Remove DP
Page: 20	Remove DP
Page: 22	from HDMI change to DP
Page: 24	Remove gpio 24 DP HPD Remove Remove gpio 18 DP HPD remove LED NET gpio 17 , from HDMI change to DP HPD
Page: 27	將 1.8V to PEX-VDD convertor
Page: 29	將 0402 MLCC*2 for L side mos
Page: 30	change PWM to I32-9509POC-U33
Page: 31	remove phase1 & phase2 driver IC
Page: 32	change phase3 driver IC to I33-536031C-T07 remove phase4
Page: 33	Remove COALY 8-PIN 6-PIN 短 接 線
Page: 36	remove 5V LED NET
Page: 37	Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1